STIC Search Report
EIC 1700

STIC Database Tracking Number: 99197

TO: Kripa Sagar
Location:
Art Unit : 1756
July 30, 2003

Case Serial Number: 09/978155

From: Barba Koroma
Location: EIC 1700
CP3/4-3D62
Phone: 305-3542

barba.koroma@uspto.gov

Search Notes

Examiner Sagar,
Please find attached completed search report as requested. The key text terms were searched in CAPLUS, COMPENDEX and WPIX databases via STN. Please let me know if you have any questions.
Thanks.

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=> file caplus
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=> file compendex
FILE 'COMPENDEX' ENTERED AT 12:29:47 ON 30 JUL 2003
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FILE COVERS 1970 TO DATE.

<<< SIMULTANEOUS LEFT AND RIGHT TRUNCATION AVAILABLE IN
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=> file wpix
FILE 'WPIX' ENTERED AT 12:29:53 ON 30 JUL 2003
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FILE LAST UPDATED:          29 JUL 2003      <20030729/UP>
MOST RECENT DERWENT UPDATE:     200348       <200348/DW>
DERWENT WORLD PATENTS INDEX SUBSCRIBER FILE, COVERS 1963 TO DATE

>>> NEW WEEKLY SDI FREQUENCY AVAILABLE --> see NEWS  <<<

>>> SLART (Simultaneous Left and Right Truncation) is now
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>>> PATENT IMAGES AVAILABLE FOR PRINT AND DISPLAY <<<
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PLEASE VISIT:
http://www.stn-international.de/training_center/patents/stn_guide.pdf <<<

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=> d que
L1 (105918) SEA FILE=CAPLUS ABB=ON PLU=ON (PHOTORESISTS OR ETCHING OR PHOTOLITHOGRAPHY)/IT
L2 (23562) SEA FILE=CAPLUS ABB=ON PLU=ON (PHOTORESIST OR PHOTOLITHOG? OR PATTERN PROFILE DISTORTION FREE)/ST
L3 (459) SEA FILE=CAPLUS ABB=ON PLU=ON (FIRST OR SECOND)(5A)PHOTORESIST
L4 (83) SEA FILE=CAPLUS ABB=ON PLU=ON FIRST(5A)SECOND(5A)PHOTORESIST
L5 (90) SEA FILE=CAPLUS ABB=ON PLU=ON FIRST(5A)SECOND(6A)PHOTORESIST
L6 (255) SEA FILE=CAPLUS ABB=ON PLU=ON FIRST(5A)SECOND(L)PHOTORESIST
L7 (6172) SEA FILE=CAPLUS ABB=ON PLU=ON PATTERN?(3A)PHOTORESIST
L8 (113567) SEA FILE=CAPLUS ABB=ON PLU=ON L1 OR L2
L9 (559) SEA FILE=CAPLUS ABB=ON PLU=ON (L3 OR L4 OR L5 OR L6)
L10 (383) SEA FILE=CAPLUS ABB=ON PLU=ON L8 AND L9
L11 (156) SEA FILE=CAPLUS ABB=ON PLU=ON L10 AND L7
L12 (66) SEA FILE=CAPLUS ABB=ON PLU=ON L11 AND (PROCESS OR METHOD)/RL
L13 (48) SEA FILE=CAPLUS ABB=ON PLU=ON SUBSTRATE AND L12
L14 (12007) SEA FILE=CAPLUS ABB=ON PLU=ON (THICK? OR DEPTH)(3A)(SUBSTRATE OR ETCHING)
L15 (1940) SEA FILE=CAPLUS ABB=ON PLU=ON L14 AND L8
L16 (4) SEA FILE=CAPLUS ABB=ON PLU=ON L15 AND L9 AND L7
L17 (52) SEA FILE=CAPLUS ABB=ON PLU=ON L16 OR L13
L18 (49) SEA FILE=CAPLUS ABB=ON PLU=ON L17 AND (PROC OR METHOD)/RL
L19 (49) SEA FILE=CAPLUS ABB=ON PLU=ON L18 AND PHOTORESIST
L20 (18) SEA FILE=CAPLUS ABB=ON PLU=ON L19 AND L6
L21 (55767) SEA FILE=COMPENDEX ABB=ON PLU=ON PHOTORESIST? OR ETCH? OR PHOTOLITHOGRAPH?
L22 (77) SEA FILE=COMPENDEX ABB=ON PLU=ON (FIRST OR SECOND)(5A)(PHOTORESIST)
L23 (77) SEA FILE=COMPENDEX ABB=ON PLU=ON L22 AND L21
L24 (24) SEA FILE=COMPENDEX ABB=ON PLU=ON L23 AND (PATTERN OR PROFILE OR DISTORT?)
L25 (1540) SEA FILE=WPIX ABB=ON PLU=ON L23 AND (PATTERN OR PROFILE OR DISTORT?)
L26 (1344) SEA FILE=WPIX ABB=ON PLU=ON L25 AND (METHOD OR PROCESS)
L27 (1056) SEA FILE=WPIX ABB=ON PLU=ON L26 AND SUBSTRATE?
L28 (34) SEA FILE=WPIX ABB=ON PLU=ON L27 AND (THICK? OR DEPTH?)(5A)SUBSTRATE

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L37          13 SEA FILE=CAPLUS ABB=ON  PLU=ON  (FIRST OR SECOND)(5A)PHOTORESIS
                T AND L20
L38          24 SEA FILE=COMPENDEX ABB=ON  PLU=ON  (FIRST OR SECOND)(5A)PHOTORE
                SIST AND L24
L39          34 SEA FILE=WPIX ABB=ON  PLU=ON  (FIRST OR SECOND)(5A)PHOTORESIST
                AND L28
L40           6 SEA FILE=CAPLUS ABB=ON  PLU=ON  L37 AND PHOTOLITHO?
L41           3 SEA FILE=COMPENDEX ABB=ON  PLU=ON  L38 AND PHOTOLITHO?
L42           4 SEA FILE=WPIX ABB=ON  PLU=ON  L39 AND PHOTOLITHO?
L43          13 DUP REM L40 L41 L42 (0 DUPLICATES REMOVED)


=> d all 1-13 l43
YOU HAVE REQUESTED DATA FROM FILE 'CAPLUS, COMPENDEX, WPIX' - CONTINUE? (Y)/N:y



L43  ANSWER 1 OF 13  CAPLUS  COPYRIGHT 2003 ACS on STN
AN   2002:522603  CAPLUS
DN   137:87038
TI   Method of forming dielectric film and dielectric film
IN   Matsuura, Masazumi
PA   Mitsubishi Denki Kabushiki Kaisha, Japan
SO   U.S. Pat. Appl. Publ., 19 pp.
     CODEN: USXXCO
DT   Patent
LA   English
IC   ICM  H01L021-31
     ICS  H01L021-469; H01L021-26; H01L021-324; H01L021-42; H01L021-477
NCL  438781000
CC   76-3 (Electric Phenomena)
FAN.CNT 1
     PATENT NO.        KIND  DATE          APPLICATION NO.  DATE
     ---------------   ----  --------      ---------------  --------
PI   US 2002090833      A1   20020711      US 2001-963648   20010927
     JP 2002203852      A2   20020719      JP 2001-627      20010105
     US 2002182891      A1   20021205      US 2002-196181   20020717
PRAI JP 2001-627        A    20010105
     US 2001-963648     A3   20010927
AB   The invention relates to a process for making a semiconductor integrated
     circuit device, comprising a first interlayer insulating film having low
     dielec. const. is formed on an underlying insulating film and a second
     interlayer insulating film is formed on the first interlayer insulating
     film.  Subsequently, a photoresist having a pattern
     with openings above regions in which copper wirings are to be formed is
     formed on the second interlayer insulating film.  Using the
     photoresist as an etching mask, the second interlayer
     insulating film and the first interlayer insulating film are
     etched, to form a recess.  Next, an ashing process using oxygen gas plasma
     is performed, to remove the photoresist.  This ashing process is
     performed under a plasma forming condition that the RF power is 300 W, the
     chamber pressure is 30 Pa, the oxygen flow is 100 sccm and the
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substrate temp. is 25 .degree. C. That provides a method of forming a dielec. film and a structure thereof, which allows suppression of a rise in dielec. const. of an interlayer insulating film, which is caused by a change of Si-CnH2n+1 bond into Si-OH bond in the film.

ST PECVD **photolithog** interlayer dielec LSI

IT Integrated circuits
Interconnections, electric
Photolithography
Photoresists
(**photolithog. patterning** of interlayer dielec. for semiconductor integrated circuit device)

IT Ashing
Etching
Vapor deposition process
(plasma; **photolithog.** patterning of interlayer dielec. for semiconductor integrated circuit device)

IT 7440-21-3, Silicon, processes 7440-50-8, Copper, processes 7631-86-9, Silica, processes 11116-16-8, Titanium nitride
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(**photolithog.** patterning of interlayer dielec. for semiconductor integrated circuit device)

L43 ANSWER 2 OF 13 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:143176 CAPLUS
DN 136:175586
TI Liquid crystal display device and method of fabricating the same
IN Kim, Jong-woo; Soh, Jae-moon; Ha, Young-hun
PA S. Korea
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
IC ICM G02F001-13
NCL 349187000
CC 74-13 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002021403	A1	20020221	US 2001-885527	20010621
PRAI KR 2000-34298	A	20000621		

AB A high yield manufg. method of fabricating an active matrix liq. crystal display is described. The method includes steps of forming a first metal layer on the **substrate** to form a gate line including a gate electrode, a gate pad, and a first capacitor electrode, forming an insulating layer, an active layer, and a second metal layer on the **substrate**, patterning the second metal layer to form a data line including a data pad, a source electrode, a drain electrode, and a second capacitor electrode, forming a passivation layer to cover the **second** metal layer, forming a **photoresist** on the passivation layer, exposing the **photoresist** using a mask having

a light shielding portion, a light transmissive portion, and a semi-transmissive portion, forming a **first photoresist** portion, a **second photoresist** portion, and a third **photoresist** portion, **patterning** the passivation layer, the active layer, and the insulating layer, and forming a pixel electrode on the passivation layer.

ST active matrix liq crystal display high manufg yield

IT Liquid crystal displays
(active matrix; high yield manufg. method for active matrix liq. crystal displays)

IT **Photolithography**
Photoresists
(high yield manufg. method for active matrix liq. crystal displays)

IT Acrylic polymers, processes
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(insulating material; high yield manufg. method for active matrix liq. crystal displays)

IT 58874-62-7
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(first metal layer; high yield manufg. method for active matrix liq. crystal displays)

IT 7440-47-3, Chromium, processes 12058-19-4, Molybdenum silicide(MoSi)
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(half-tone mask; high yield manufg. method for active matrix liq. crystal displays)

IT 7439-98-7, Molybdenum, processes
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(high yield manufg. method for active matrix liq. crystal displays)

IT 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes 124221-30-3, BCB
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(insulating material; high yield manufg. method for active matrix liq. crystal displays)

L43 ANSWER 3 OF 13 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:655057 CAPLUS
DN 137:193842
TI Method of forming dual damascene structure
IN Liu, Chih-chien; Huang, Jui-tsen; Cheng, Yi-fang; Yang, Ming-sheng
PA United Microelectronics Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-302
NCL 438706000
CC 76-3 (Electric Phenomena)

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6440861	B1	20020827	US 2000-652471	20000831
PRAI	TW 2000-89116603	A	20000817		

AB A method of forming a dual damascene structure. A **first** dielec. layer and a **second** dielec. layer are sequentially formed over a **substrate**. A **first photoresist** layer is formed over the **second** dielec. layer. **Photolithog.** and etching operations are conducted to remove a portion of the **second** dielec. layer and the **first** dielec. layer so that a via opening is formed. A conformal third dielec. layer is coated over the surface of the second dielec. layer and the interior surface of the via opening. The conformal third dielec. layer forms a liner dielec. layer. A **second photoresist** layer is formed over the **second** dielec. layer and then the **second photoresist** layer is **patterned**. Using the **patterned second photoresist** layer as a mask, a portion of the second dielec. layer is removed to form a trench. The **patterned second photoresist** layer is removed. Conductive material is deposited over the **substrate** to fill the via opening and the trench. Finally, chem.-mech. polishing is conducted to remove excess conductive material above the second dielec. layer.

ST dual damascene semiconductor integrated circuit

IT Vapor deposition process
(chem.; fabrication of dual damascene structure semiconductor integrated circuit)

IT **Etching**
Integrated circuits
Interconnections, electric
Photolithography
Photoresists
(fabrication of dual damascene structure semiconductor integrated circuit)

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
203945-07-7, SiLK
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(fabrication of dual damascene structure semiconductor integrated circuit)

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD

RE

(1) Andricacos; US 6268291 B1 2001 CAPLUS
(2) Anon; JP 2000208745 A 2000 CAPLUS
(3) Givens; US 6271593 B1 2001
(4) Jang; US 6268294 B1 2001 CAPLUS
(5) Li; US 6040243 A 2000 CAPLUS

L43 ANSWER 4 OF 13 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN

AN 2002-403374 [43] WPIX

DNN N2002-316484 DNC C2002-113383

TI Manufacture of phase shifting mask by forming phase shifter layer and

opaque shield layer on **substrate**, defining the layers, performing **etching** procedure, and performing cleaning procedure to **tch** portion of phase shifter surface.

DC L03 U11
IN CHANG, C
PA (CHAN-I) CHANG C
CYC 1
PI US 2002030034 A1 20020314 (200243)* 8p B29D011-00
ADT US 2002030034 A1 US 2000-726459 20001130
PRAI TW 2000-118676 20000913
IC ICM B29D011-00
ICS C03C015-00; C03C025-68; C23F001-00; C23F003-00; C25F003-00
AB US2002030034 A UPAB: 20020709
NOVELTY - Phase shifting mask is manufactured by forming sequentially a phase shifter layer (202) and an opaque shield layer (204) on a **substrate** (200); defining the layers; performing an **etching** procedure, **etching** the **substrate** and exposing its portion, and **etching** the **substrate** to a predetermined **depth** (210); and performing a cleaning procedure that **etches** a portion of the phase shifter surface.

DETAILED DESCRIPTION - Manufacture of phase shifting mask comprises forming sequentially a phase shifter layer and an opaque shield layer on a **substrate**; defining the layers, respectively; performing an **etching** procedure, **etching** the **substrate** and exposing its portion, and **etching** the **substrate** to a predetermined **depth**; and performing a cleaning procedure that **etches** a portion of the phase shifter surface, where the predetermined depth is based on an **etched** thickness (212) of the phase shifter layer.

USE - The **method** is used to manufacture a phase shifting mask that is used to raise the resolution of **pattern** transfer during a **photolithographic** procedure.

ADVANTAGE - The phase difference between the **substrate** and the phase shifter layer stays the same before and after washing or repair **process**.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view that illustrates a **method** of manufacturing a phase shift mask.

Substrate 200
Phase shifter layer 202
Opaque shield layer 204
Predetermined depth 210
Etched thickness 212

Dwg.2E/2
FS CPI EPI
FA AB; GI
MC CPI: L04-C06A
EPI: U11-C04E2

L43 ANSWER 5 OF 13 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-413477 [44] WPIX
DNN N2002-324942 DNC C2002-116829
TI Manufacture of semiconductor device involves **etching**

second dielectric layer using developed **photoresist** and **etching first** dielectric layer and **etch**-stop layer using the second dielectric layer.

DC L03 U11 U14

IN PLAT, M V; SHEN, L; SUBRAMANIAN, R; YANG, W

PA (ADMI) ADVANCED MICRO DEVICES INC

CYC 1

PI US 6365509 B1 20020402 (200244)* 13p H01L021-4763

ADT US 6365509 B1 US 2000-586556 20000531

PRAI US 2000-586556 20000531

IC ICM H01L021-4763
ICS H01L021-302; H01L021-311; H01L021-461

AB US 6365509 B UPAB: 20020711

NOVELTY - A semiconductor device is manufactured by depositing sequentially an **etch**-stop layer, first and **second** dielectric layers and a **photoresist** on a **substrate**. The **photoresist** is patterned, processed and developed. The second dielectric layer is **etched** using the developed **photoresist**. The **first** dielectric layer and **etch**-stop layer are **etched** using the second dielectric layer.

DETAILED DESCRIPTION - Manufacture of a semiconductor device involves depositing sequentially an **etch**-stop layer (418), a first dielectric layer, a **second** dielectric layer and a **photoresist** (424) on a semiconductor **substrate** (402). The **photoresist** has a **thickness** of less than twice the thickness of the of the second dielectric layer. It is patterned, **photolithographically** processed and developed. The second dielectric layer is **etched** using the developed **photoresist**. The **first** dielectric layer is **etched** using the **second** dielectric layer so that the **photoresist** and the **first** dielectric layer are **etched** with a portion of the second dielectric layer. The **etch**-stop layer is **etched** using the second dielectric layer so that the remaining layer of the second dielectric layer and the **etch**-stop layer are **etched**.

USE - For manufacturing a semiconductor device, e.g. flash electrically erasable programmable read only memories.

ADVANTAGE - The inventive **method** minimizes variation in the **etching process** by using the silicon oxynitride as a bottom anti-reflective layer (422) and hard mask in conjunction with a thin **photoresist** layer. The thin **photoresist** also allows for less variation in the **photolithographic process**.

DESCRIPTION OF DRAWING(S) - The figure illustrates the sequence of **process** steps of a **process** for forming an interconnect structure and its connected contact on semiconductor **substrate**.

Substrate 402
Etch-stop layer 418
Bottom anti-reflective layer 422
Photoresist 424

Dwg.4/4

FS CPI EPI

FA AB; GI
MC CPI: L03-G04A; L04-C06B; L04-C07; L04-C12
EPI: U11-C18B5; U14-A03B7

L43 ANSWER 6 OF 13 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2001:817079 CAPLUS
DN 135:350566
TI Use of rapid thermal annealing furnace for **photoresist** baking
IN Subramanian, Ramkumar; Rangarajan, Bharath; Templeton, Michael K.; Singh, Bhanwar
PA Advanced Micro Devices, Inc., USA
SO PCT Int. Appl., 16 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM G03F007-38
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001084243	A1	20011108	WO 2001-US10925	20010403
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	US 6335152	B1	20020101	US 2000-564408	20000501
	EP 1282839	A1	20030212	EP 2001-924657	20010403
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
	TW 480575	B	20020321	TW 2001-90110316	20010430
PRAI	US 2000-564408	A	20000501		
	WO 2001-US10925	W	20010403		

AB In one embodiment, the present invention relates to a method of processing an irradiated **photoresist** involving the steps of placing a **substrate** having the irradiated **photoresist** thereon (1) at a **first** temp. in a rapid thermal anneal furnace; heating the **substrate** (1) to a second temp. within about 0.1 s to about 10 s; cooling the **substrate** (1) to a third temp. in a rapid thermal annealing furnace (21) within about 0.1 s to about 10 s; and developing the irradiated **photoresist**, wherein the **second** temp. is higher than the **first** temp. and the third temp. In another embodiment, the present invention relates to a system of processing a **photoresist**, contg. a source of actinic radiation and a mask of selectively irradiating a **photoresist**; a rapid thermal annealing furnace for rapidly heating and rapidly cooling a selectively irradiated **photoresist**, wherein the rapid heating and rapid cooling are

independently conducted within about 0.1 s to about 10 s; and a developer for developing a rapid thermal annealing furnace heated and selectively irradiated **photoresist** into a **patterned** **photoresist**. The object of the present invention is to improve crit. dimension control of **photoresist** processing.

ST **photoresist** baking rapid thermal annealing furnace

IT Electric furnaces
(heat-treatment; use of rapid thermal annealing furnace for **photoresist** baking)

IT **Photolithography**
Rapid thermal annealing
(use of rapid thermal annealing furnace for **photoresist** baking)

IT 7782-42-5, Graphite, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); **PROC (Process)**; USES (Uses)
(use of rapid thermal annealing furnace for **photoresist** baking)

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD

RE

(1) Anon; PATENT ABSTRACTS OF JAPAN 1983, V007(078), PP-188
(2) Anon; PATENT ABSTRACTS OF JAPAN 1986, V010(016), PE-375
(3) Fujitsu Ltd; EP 0103052 A 1984
(4) Matsuoka, Y; US 4946764 A 1990
(5) Nippon Denshin Denwa Kosha; JP 58009141 A 1983 CAPLUS
(6) Okamura, K; US 5849602 A 1998 CAPLUS
(7) Shigemitsu, F; US 4840874 A 1989 CAPLUS
(8) Toshiba Kk; JP 60178626 A 1985 CAPLUS
(9) Toshiba Kk; JP 61080247 A 1986 CAPLUS
(10) Wieland, R; US 5302495 A 1994 CAPLUS

L43 ANSWER 7 OF 13 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN

AN 2001-202077 [20] WPIX

DNN N2001-144100 DNC C2001-059947

TI Production of monolithic optical microbench for coupling of light between optical devices by forming curved reflective mirror and groove by **etching**, cleaning the surfaces and metallizing the entire **substrate** wafer.

DC L03 P81 U11 U12 U13 V07

IN ANDERSON, E R; REZEK, E A; STRIJEK, R L; TRAN, D

PA (THOP) TRW INC

CYC 2

PI	US 6187515	B1 20010213 (200120)*	13p	G02B006-36
	JP 11344632	A 19991214 (200120)	10p	G02B006-122
	JP 3143450	B2 20010307 (200122)	9p	G02B006-122

ADT US 6187515 B1 US 1998-74188 19980507; JP 11344632 A JP 1999-127712 19990507; JP 3143450 B2 JP 1999-127712 19990507

FDT JP 3143450 B2 Previous Publ. JP 11344632

PRAI US 1998-74188 19980507

IC ICM G02B006-122; G02B006-36
ICS G02B006-42; H01L033-00; H01S003-18

AB US 6187515 B UPAB: 20010410

NOVELTY - A monolithic optical microbench is made by selectively aligning first and second masks to respective first and second surfaces of a **substrate** wafer; exposing the surfaces coated with **first** and **second** layers of **photoresist** material to a light source; forming a curved reflective mirror and a groove by **etching** ; cleaning the surfaces; and metallizing the entire **substrate** wafer.

DETAILED DESCRIPTION - Production of a monolithic optical microbench for the coupling of light between optical devices includes providing a III-V semiconductor **substrate** wafer having first and second opposing surfaces, and first and second crystal planes. The entire first surface of the **substrate** wafer is lapped and polished. **First** and **second** layers of **photoresist** material are coated over the entire first and second opposing surfaces of the **substrate** wafer, respectively. The **first** and **second** layers of **photoresist** material is baked at 150 deg. C. First and second masks are provided for the first and second opposing surfaces, respectively. They are selectively aligned to the first and second opposing surfaces of the **substrate** wafer, respectively. The first and second opposing surfaces coated with the **first** and **second** layers of **photoresist** material are exposed to a light source to form **first** and **second photoresist** masks, respectively. The **first** and **second** opposing surfaces are developed. The first opposing surface is **etched** at 60-65 deg. C to form a curved reflective mirror. The second opposing surface is **etched** to form a groove (82) intersecting a plane of the curved reflective mirror (66). The **first** and **second photoresist** masks are removed and the **first** and second opposing surfaces are cleaned. The entire **substrate** wafer (48) is metallized.

USE - For producing monolithic optical microbench for the coupling of light between optical devices.

ADVANTAGE - The microbench can be made of the same semiconductor material of the device, thus there is a better thermal expansion match between the microbench and the micro-optical devices. The invention provides redirection and focusing of optical energy using one optical component, lower loss and spherical aberrations using front surface reflectors compared to refractive lenses, compact construction and reduced package **profile**, very accurate alignment of reflector to optical devices, decrease in the time required for alignment of the reflector to the micro-optical device by passive alignment, and expandability to integrate reflectors into one structure. It provides for more efficient packaging of optical electronics systems. Finally, very precise fabrication is possible by using standard **photolithography processes** and wafer level fabrication can result in high volume manufacturing and high reproducibility. The monolithic integration allows for more reliable and accurate alignment between optical devices.

DESCRIPTION OF DRAWING(S) - The figure shows a **substrate** wafer metallization **process**.

Entire **substrate** wafer 48

Reflective mirror 66

Groove 82

Titanium layer 86
Platinum layer 88
Gold layer 90
Evaporating 92
Dwg.5m/7
FS CPI EPI GMPI
FA AB; GI
MC CPI: L03-G02
EPI: U11-F02B; U12-A01C; U13-D04A; V07-F01A5; V07-G10C; V07-G10D

L43 ANSWER 8 OF 13 COMPENDEX COPYRIGHT 2003 EEI on STN
AN 2000(40):7006 COMPENDEX
TI Nanopatterning of organic and inorganic materials by holographic lithography and plasma **etching**.
AU Visconti, P. (Universita di Lecce, Lecce, Italy); Turco, C.; Rinaldi, R.; Cingolani, R.
MT 25th International Conference on Micro- and Nano-Engineering.
ML Rome, Italy
MD 21 Sep 1999-23 Sep 1999
SO Microelectronic Engineering v 53 n 1 Jun 2000.p 391-394
CODEN: MIENEF ISSN: 0167-9317
PY 2000
MN 57178
DT Journal
TC Application; Experimental
LA English
AB We report on the nanopatterning of semiconductors and conjugated polymers to produce photonic band gap structures. Poly(p-phenylenevinylene) (PPV) thin films prepared by spin coating on ITO-coated glass, GaAs and Si substrates were successfully processed. The technological process for the patterning was based on U.V.holographic lithography (364 nm line of Ar plus Laser) and plasma **etching**. **First** a **photoresist** layer was deposited on the sample surface and exposed to an interference **pattern** in a 'corner cube' interferometer, with multiple exposure capability, in order to realize **pattern** of lines, squares, pillars and holes. The shape of the pillars and holes, produced by double exposure, can be changed by rotating the sample by angles in the range between 30 and 90 degrees.Each step in the mask production procedure was carefully controlled by AFM measurements. Then the **photoresist patterns** were transferred to the substrate materials by means of a plasma **etching** in a parallel plate reactor. In the case of PPV, a long optimization of the Argon plasma parameters was done in order to balance the **photoresist** versus PPV **etching** rate and to prevent over-**etching** of the PPV. This problem is inherent to the organic nature and similar chemical characteristics of the two materials and it makes the mask transfer process in the PPV very critical. The resulting patterned region consisted of 200nm wide parallel lines with a periodicity of 400nm in the case of single exposure, whereas ordered two dimensional arrays of pillars (250nm in diameter) were produced with a double exposure of the **photoresist** mask. A CH4/H2/Ar and CF4 based reactive ion **etching** was used to transfer the 2D holographic

photoresist patterns respectively to the substrates of GaAs and Si, in order to realize two-dimensional matrices of pillars and holes for photonic band-gap applications and optical devices based on matrices of dots or anti-dots. (Author abstract) 7 Refs.

CC 714.2 Semiconductor Devices and Integrated Circuits; 712.1 Semiconducting Materials; 815.1.1 Organic Polymers; 743.1.1 Optical Holography; 932.3 Plasma Physics; 712.1.2 Compound Semiconducting Materials

CT ***Photoresists**; Masks; **Photolithography**; Holography; Plasma **etching**; Thin films; Semiconducting gallium arsenide; Semiconducting silicon; Semiconductor materials; Organic polymers

ST Holographic lithography; Polyphenylenevinylene thin films; **Photoresists patterns**; Photonic band gap structures

ET As*Ga; As sy 2; sy 2; Ga sy 2; GaAs; Ga cp; cp; As cp; Si; Ar; C*H; CH4; C cp; H cp; C*F; CF4; F cp; D

L43 ANSWER 9 OF 13 CAPLUS COPYRIGHT 2003 ACS on STN

AN 2000:496407 CAPLUS

DN 133:82830

TI Fabrication of semiconductor device from aluminum

IN Na, Kwan-Koo

PA LG Semiconductor Co., Ltd., S. Korea

SO Repub. Korea, No pp. given
CODEN: KRXXFC

DT Patent

LA Korean

IC ICM H01L021-302

CC 76-3 (Electric Phenomena)

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 9613140	B1	19960930	KR 1988-3382	19880328
PRAI	KR 1988-3382		19880328		

AB The method of fabricating semiconductor device comprises the steps of: forming an oxide film on a semiconductor **substrate** and a first Al layer pattern on the oxide film; forming a PIQ layer on the oxide film and on the **first** Al **pattern** and a **photoresist** layer on the PIQ layer; forming a **photoresist pattern**; forming a mask metal layer on the **photoresist pattern** and forming a mask metal layer **pattern** by removing the **photoresist pattern**; exposing the **first** Al pattern by etching the PIQ layer; and forming a **second** Al layer connecting the **first** Al layer pattern.

ST semiconductor device manuf aluminum

IT Semiconductor device fabrication
Semiconductor devices
(fabrication of semiconductor device from aluminum)

IT Metals, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(film; fabrication of semiconductor device from)

IT Oxides (inorganic), uses
RL: DEV (Device component use); SPN (Synthetic preparation); PREP

(Preparation); USES (Uses)
(films; fabrication of semiconductor device from)
IT **Etching**
Etching masks
Photolithography
(in fabrication of semiconductor device from aluminum)
IT Semiconductor materials
(**substrate**; in fabrication of semiconductor device from aluminum)
IT 7429-90-5, Aluminum, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(fabrication of semiconductor device from)

L43 ANSWER 10 OF 13 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2000:473005 CAPLUS
DN 133:67276
TI Method for manufacturing a storage node of semiconductor memory device
IN Seo, Jae-bum
PA Lg Semiconductor Co., Ltd., S. Korea
SO Repub. Korea, No pp. given
CODEN: KRXXFC
DT Patent
LA Korean
IC ICM H01L027-108
ICS H01L027-10
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI KR 9605568	B1	19960426	KR 1992-21881	19921120
PRAI KR 1992-21881		19921120		

AB The method includes the steps of : forming a first oxide layer and nitride layer, in series, on a semiconductor **substrate**, a storage node contact through **photolithog.**, and forming a **first** polysilicon layer and **second** oxide layer, in series, on the **substrate** and forming a **photoresist pattern** thereon, wet-etching the **second** oxide layer by using the **photoresist pattern** as a mask to form oxide protrusion narrower than the **photoresist pattern** width around the storage node contact; forming a polysilicon sidewall on the sides of the protrusion, etching the **second** oxide layer and **first** polysilicon layer by using the polysilicon sidewall as a mask to form a cylinder of the second oxide layer; removing the portion of the second oxide layer placed between the cylinders; and forming a polysilicon sidewall on the side of the cylinder structure, thereby forming a storage node in the shape of double cylinder.
ST storage node semiconductor memory device fabrication
IT **Etching**
Etching masks
Photolithography
(in method for manufg. a storage node of semiconductor memory device)

IT Semiconductor device fabrication
Semiconductor memory devices
(method for manufg. a storage node of semiconductor memory device)
IT 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(in method for manufg. a storage node of semiconductor memory device)
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); **PROC (Process)**; USES (Uses)
(poly; in method for manufg. a storage node of semiconductor memory device)

L43 ANSWER 11 OF 13 COMPENDEX COPYRIGHT 2003 EEI on STN
AN 1996(40):65 COMPENDEX
TI Binary gratings for CO2 laser-beam diagnostics.
AU Hembd-Sollner, Ch. (Inst fuer Technische Optik, Stuttgart, Ger); Budzinski, Ch.; Tiziani, H.
SO Applied Optics v 35 n 19 Jul 1 1996.p 3662-3670
CODEN: APOPAI ISSN: 0003-6935
PY 1996
DT Journal
TC Theoretical; Experimental
LA English
AB Presented are the results concerning binary gratings for CO2 lasers. The layout proposed by Loewen et al.(1976) has for the first time to the authors' knowledge been realized by galvanic technology. This method, which preserves polarization of the diagnostic beam, is extended to focusing gratings. The diffractive structures were fabricated in **photoresist** in a **first** step. Because high-power densities damage occurs in resist, the structures were transferred in a second step by electroforming into upper substrates.Numerical calculations are carried out by a modal theory. The appearance of Rayleigh anomalies is demonstrated.24 Refs.
CC 741.3 Optical Devices and Systems; 744.2 Gas Lasers; 744.8 Laser Beam Interactions; 921.6 Numerical Methods; 544.1 Copper; 745.1 Printing
CT *Diffraction gratings; **Photolithography**; Modal analysis; Light absorption; Boundary conditions; Diffraction; Calculations; Copper; Carbon dioxide lasers; Laser beams
ST Binary gratings; Laser beam diagnostics; Modal theory; Elliptical beam **distortion**; Rayleigh anomalies; Impedance boundary conditions
ET C*O; CO2; C cp; cp; O cp

L43 ANSWER 12 OF 13 COMPENDEX COPYRIGHT 2003 EEI on STN
AN 1997(37):4658 COMPENDEX
TI Scatterometry for 0.24-0.70 um developed **photoresist** metrology.
AU Murnane, Michael R. (Univ.of New Mexico, Albuquerque, NM, USA); Raymond, Christopher J.; Prins, Steven L.; Naqvi, S.Sohail H.; McNeil, John R.
MT Integrated Circuit Metrology, Inspection, and Process Control IX.
MO SPIE - Int Soc for Opt Engineering, Bellingham, WA USA
ML Santa Clara, CA, USA
MD 20 Feb 1995-22 Feb 1995

SO Proceedings of SPIE - The International Society for Optical Engineering v 2439 1995.Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA.p 427-436
CODEN: PSISDG ISSN: 0277-786X
ISBN: 0-8194-1787-4
PY 1995
MN 22267
DT Conference Article
TC Application; Theoretical; Experimental
LA English
AB Scatterometry, the characterization of periodic structures via diffracted light analysis, is shown to be a viable and versatile metrology for critical dimensions as small as 0.24 mu m. Scatterometry is rapid, nondestructive, inexpensive, and potentially useful for on- line control during several microlithographic processing steps.This paper discusses two recent studies in which scatterometry was applied to the measurement of developed **photoresist patterns.First**, scatterometric measurements of developed resist lines in the 0.38 mu m to 0.70 mu m range will be presented.Results from four sample wafers are shown to be consistent with SEM measurements.For one wafer, the average deviation of scatterometry linewidth measurements form top-down SEM measurements, over a broad exposure range, is 14.5 nm.Moreover, our scatterometer is shown to be highly linear with the SEM; linearity coefficients have typically been above 0.99.The goal of our second project has been to determine whether scatterometry measurements are affected by variations in the integrated circuit production process.A set of twenty-five wafers was fabricated with deliberate variations in the exposure dose and the underlying film thicknesses.We are presently investigating the effects of the film thicknesses on the measurements of critical dimensions (CDs) as small as 0.24 mu m.Preliminary results indicate that CDs and multiple thin films can be simultaneously measured by applying multi-parameter prediction algorithms to the scattered light data. Results from four different prediction algorithms are given. Finally, the repeatability of the scatterometer is shown to be excellent: 0.5 nm for consecutive measurements and 0.8 nm for day-to-day measurements.The results of an extensive repeatability/precision experiment are presented.14 Refs.
CC 745 Printing and Reprography; 817.1 Plastics Products; 731.3 Specific Variables Control; 741.1 Light. Optics; 941.3 Optical Instruments; 941.4 Optical Variables Measurements
CT ***Photolithography**; Process control; **Photoresists**; Signal filtering and prediction; Light scattering; Measurements
ST **Photoresist** metrology; Scatterometric linewidth measurement; Critical dimension measurement; Multi-parameter prediction algorithm

AN 1990-157331 [21] WPIX
DNN N1990-122302 DNC C1990-068460
TI Sub-micron structured mask prodn. - by combination of sidewall technology and **photolithography**.
DC A85 L03 P84 U11
IN KOBLINGER, O; MEISSNER, K; MUHL, R; TRUMPP, H J; ZAPKA, W

PA (IBMC) IBM CORP
CYC 5
PI EP 369053 A 19900523 (199021)*
R: DE FR GB
JP 02251849 A 19901009 (199046)
US 5055383 A 19911008 (199143)
EP 369053 B1 19940302 (199409) DE 16p H01L021-00
R: DE FR GB
DE 3888184 G 19940407 (199415) H01L021-00
JP 08027533 B2 19960321 (199616) 7p G03F001-08
ADT EP 369053 A EP 1988-119094 19881117; JP 02251849 A JP 1989-297815 19891117; US 5055383 A US 1989-420870 19890812; EP 369053 B1 EP 1988-119094 19881117; DE 3888184 G DE 1988-3888184 19881117, EP 1988-119094 19881117; JP 08027533 B2 JP 1989-297815 19891117
FDT DE 3888184 G Based on EP 369053; JP 08027533 B2 Based on JP 02251849
PRAI EP 1988-119094 19881117
REP EP 10624; EP 111086; EP 223032; EP 280587; US 4331708; US 4354896; US 4648937
IC G03F001-08; H01L021-76
ICM G03F001-08; H01L021-00
ICS H01L021-027; H01L021-76
AB EP 369053 A UPAB: 19930928
Masks with submicron-size structures are produced by (a) applying a first insulating layer (sequence) (2) onto a silicon **substrate** (1); (b) applying a **photoresist** or polymer-layer (3) and removing parts of the layer to form structure (7) with horizontal and vertical surfaces; (c) applying a second insulating layer onto the horizontal and vertical surfaces and the exposed regions of the first insulating layer (2); (d) planarising the structure by applying a **photoresist** or polymer material and back-**etching** until the start of the vertical flanks of the sidewall covering the second insulating layer on the structures (7) is exposed; (e) **photolithographically** producing a trimming mask, covering desired regions of the second insulating layer; (f) removing hte-esthe exposed regions of the second insulating layer by isotropic **etching**; (g) transferring the dimensions (A-B) of the resulting openings, defined by the vertical surfaces of the **photoresist** or polymer structure, to the **first** insulating layer (2) by anisotropic **etching**; (h) **etching** away the trimming mask, the planarised resist or polymer material, the resist or polymer structure (7) and the remainder of the second insulating layer; (i) depositing a further **photoresist** layer on the **first** insulating layer (2) and **photolithographically** processing to produce a **pattern** of openings for line widths greater than 0.5 microns; (j) transferring this **pattern** onto the first insulating layer by anisotropic **etching**; (k) producing trenches of desired **depth** in the silicon **substrate** (1) by anisotropic **etching** using the first insulating layer as mask; and (l) removing the first insulating layer (2) by wet **etching**.
2/9
FS CPI EPI GMPI
FA AB; GI

MC CPI: A11-B05; A11-C04D; A11-C04E; A12-L02B2; L04-C06A
EPI: U11-C04A4